ALLEN WATERS
Oregon State University

Degrees:

- Honors Bachelor of Science, Electrical and Computer Engineering (June 2010)
- PhD, Electrical and Computer Engineering (tentatively June 2014)

Scholar Donors:

Portland ARCS Chapter Scholar Award

About the Scholar:

Allen is researching minimalist and synthesizable analog-to-digital converter architectures that would allow the same digital automation tools used in digital circuit design to be applied to analog and mixed-signal circuits. As semiconductor processes scale, digital circuits benefit from reduced power and area, and increased speed. Analog circuits suffer from reduced intrinsic gain and reduced supply range; noise performance worsens. In order to continue scaling into submicron processes, digital-like architectures are used; furthermore, techniques such as oversampling and stochastic conversion are used to improve tolerance to device mismatch.

Benefits to Society:

There are two major benefits from synthesizable analog-to-digital conversion: first, analog circuit design will continue to scale into smaller and lower-power technologies. In addition to the obvious reduction in power consumption, smaller area would translate into improvements in biomedical sensor applications- less obtrusive sensors and test equipment for these sensor applications.

Second, because the layout process is automated, the time required to implement a design rapidly decreases. This would shorten the design process, saving time and money. More importantly, it puts the important biomedical sensors in the hands of people who need them faster. Both the scalability and synthesizability of the ADC design will have benefits to quality of life.

Awards and Honors:

- Drucilla Shephard Smith Scholastic Award
- J&C Mathes Scholarship
- School of EECS Sophomore of the Year Award
- National Merit Scholarship

Publications and Posters:

- J. Guerber, M. Gande, H. Venkatram, **A. Waters**, U. Moon, “A 10b Ternary SAR ADC with Quantization Time Information Utilization,” *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2604-2613, Nov. 2012.
- J. Guerber, M. Gande, H. Venkatram, **A. Waters**, U. Moon, “A 10b Ternary SAR ADC with Decision Time Quantization Based Redundancy,” *IEEE Asian Solid-State Circuits Conf.*, Nov. 2011, pp. 65-68.