Analog-to-Digital Data Converter Design

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Context and Background

The *analog-to-digital converter* (ADC) has widespread usage in almost all technology today. Anything which interfaces with the real world and processes information requires an ADC.


Medical Devices


Consumer and Home Electronics

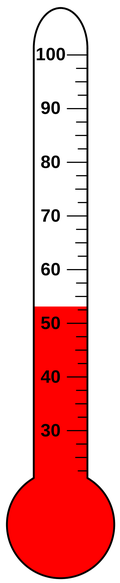
5G Communication


Autonomous Vehicles

As an example:

The conversion of an analog signal… to a digital one!

Temperature Example



Actual Temperature (Analog)	Thermometer (Digital)
53.1250	52.5, error of 0.625

In terms of data-converter terminology:

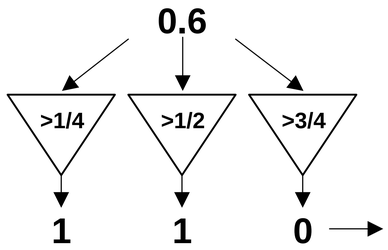
This thermometer has:
32 levels (5 bits 30dB Signal-to-Noise Ratio)
Only reads non-moving signals (D.C.)

In contrast, todays modern converters have:
Up to 120dB SNR (over 1 million levels)
Up to 10's of giga-samples per second
(one measurement every 1/10th of a nanosecond)

For reference, imagine a scale that can measure the weight of a fully loaded Airbus A380, accurate to the pound, before light travels 1.2 inches.

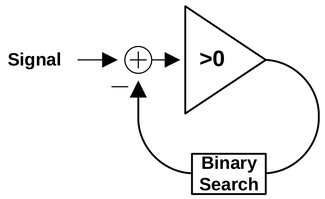
All Different Kinds of Converters!

Flash



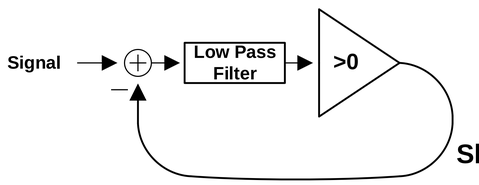
Utilizes many comparisons at once to compare an input to many different reference levels. Very fast but power hungry.

Successive Approximation Register (SAR)



Utilizes a single comparator and a binary search algorithm. Slower than flash, but power efficient.

ΔΣ (Delta-Sigma)

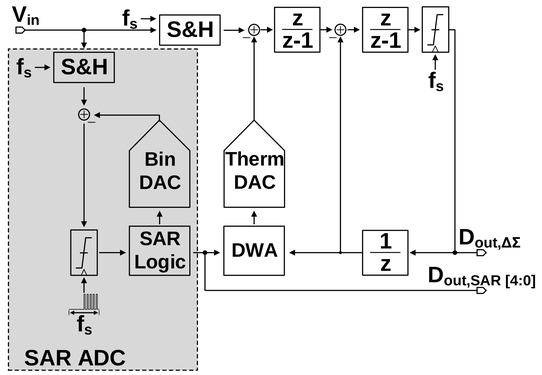


Utilizes filtering before making comparisons. Slow but extremely accurate.

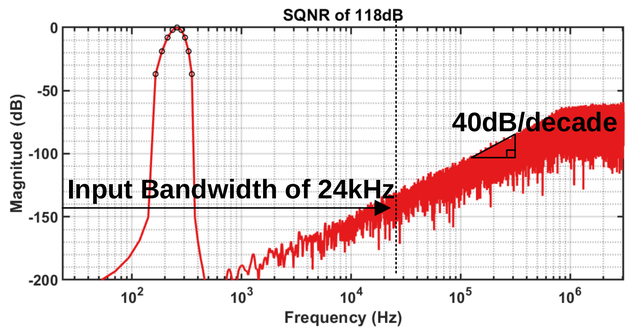
There are many other varieties of data-converters. Some are hybrid structures of the ones shown here. Others are made with a chain of converters. Each converter has its own strengths and weaknesses.

Current Research

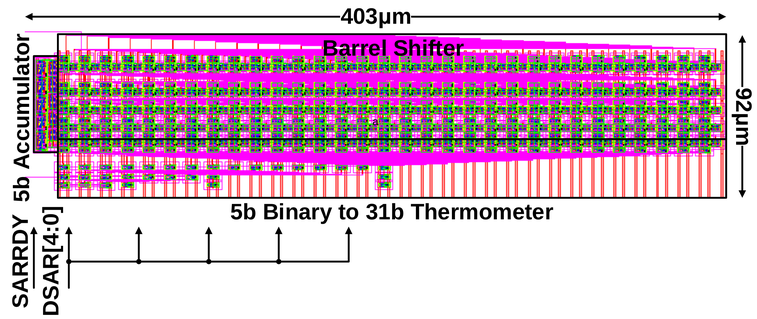
Zoom ADC (0-2 MASH)



ADC Dynamic Output Spectrum



Data Weighted Averaging (DWA) Circuit



Converter Design Timeline: 9 to 36 months

Research Survey and Ideas	Design	Layout	Fabrication	Testing and Evaluation
1 to 4 months	3 to 18 months	2 to 6 months	2 to 3 months	1 to 5 months

A typical PhD student at OSU does 2 to 3 chips involving some or all of these steps

Publications

- A. ElShater, C. Y. Lee, P. K. Venkatachala, J. Muhlestein, S. Leuenberger, K. Sobue, K. Hamashita, U-K. Moon "A 10mW 16b 15MS/s Two-Step SAR ADC wth 95dB DR Using Dual-Deadzone Ring-Amplifier," *IEEE Int. Solid-State Circuits Conf.* (ISSCC), Feb 2019
- C. Lee, S. Leuenberger, P. Venkatachala, A. ElShater, M. Oatman, B. Xiao, U. Moon "A power efficient SAR algorithm for high resolution ADCs," *IEEE Int. Symp. Circuits Syst.* (ISCAS), May 2018
- P. Venkatachala, S. Leuenberger, A. ElShater, C. Lee, Y. Xu, B. Xiao, M. Oatman, U. Moon "Process invariant biasing of ring amplifiers using deadzone regulation circuit," *IEEE Int. Symp. Circuits Syst.* (ISCAS), May 2018
- P. Venkatachala, S. Leuenberger, A. ElShater, C. Lee, J. Muhlestein, B. Xiao, M. Oatman, U. Moon "Passive compensation for improved settling and large signal stabilization of ring amplifiers," *IEEE Int. Symp. Circuits Syst.* (ISCAS), May 2018
- S. Leuenberger, P. Venkatachala, A. ElShater, M. Oatman, C. Lee, B. Xiao, U. Moon "The impact of dynamic bandwidth of ring amplifiers on analog-to-digital converter design," *IEEE Int. Symp. Circuits Syst.* (ISCAS), May 2018
- B Xiao, S. Leuenberger, P. Venkatachala, A. ElShater, C. Lee, M. Oatman, and U. Moon, "Power optimized comparator selecting method For stochastic ADC," *IEEE Int. Symp. Circuits Syst.* (ISCAS), May 2018